

Your ESD / IO Design Experts

SEVICES

ESD / IO design
Special Analog IOs, e.g. RF
ESD Consulting

PRODUCT IO Libraries

Standard IO libraries
Template IO libraries
Fully Customized IO libraries
Design of Analog RF-IOs

ESD/IO IP

Si-proven in CMOS
180nm to 45nm
Product proven in 100s of ICs
Foundry proven incl. TSMC
Fully portable
Simulation verified ESD in
product specific designs

CONTACT

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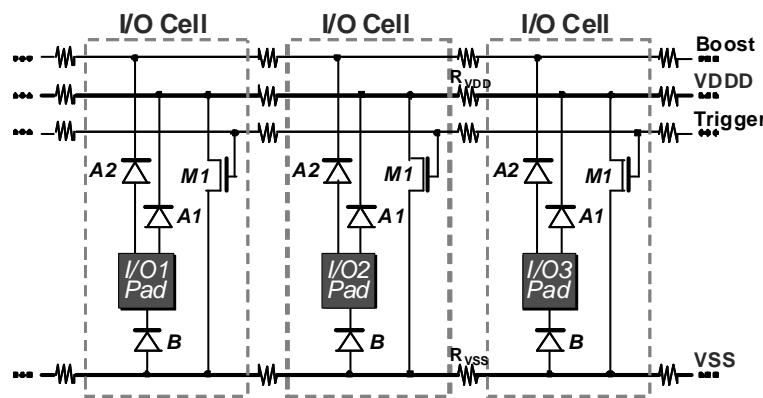
About Certus

Certus Semiconductor is a global company, founded by a collaborating team of world renowned experts in both ESD and IO design. Certus is offering the semiconductor industry a new approach to custom IO libraries, including tailored IO designs, and ESD solutions based on simulation that leverage specialized silicon ESD models.

The technique enables fully silicided NMOS devices in output drivers thus consuming less area, capacitance, resistance – ideal for high-speed applications. The highly efficient ESD design technique includes a SPICE simulation and optimization process that guarantees a highest confidence level for IC qualification even for the highly package dependent CDM specification.

IO Cell Library Offerings

Certus is offering their customers new options for IO design. In addition to the standard “off the shelf” IO libraries provided by many foundries and IP companies, Certus, is offering flexible IO template libraries.



ESD protection design applying a distributed, boosted rail-clamp network

ESD Design Methodology

Certus has acquired rights and licenses to market and distribute ESD and IO design IP, based upon Freescale’s class leading proprietary ESD/IO technology. The unique ESD/IO design concept applies a distributed and boosted rail-clamp network for most uniform and thus efficient ESD protection along an IO bank.

An IO cell template defines the cell physical architecture and includes the cell frame, pads, power bussing, ESD circuitry, etc. – that is everything except for the functional I/O circuitry. In addition to the IO cell template, a complete I/O template library includes the full set of required power/ground cells, filler/cut cells and corner cells.

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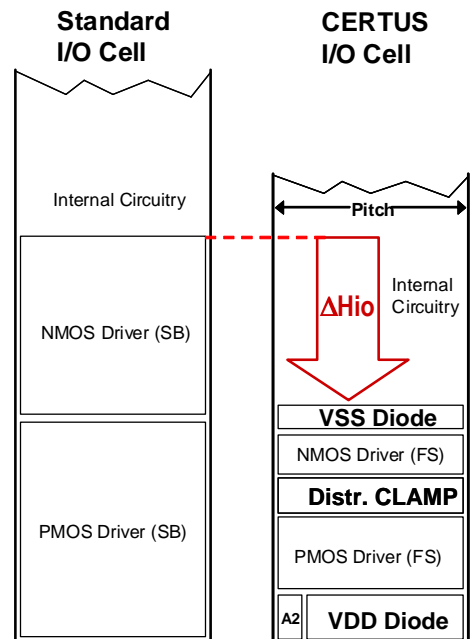
concentrate on what they do best. The IO template libraries allow our custom functional IO design, while IC design customers to leaving the process technology concentrate on what they do best - specific challenges of robust ESD custom functional IO design - while and physical architecture definition the process technology specific to Certus. These template library challenges of robust ESD and offerings allow our customers to physical architecture definition is create fully custom IO libraries in left to Certus. With the template an amazingly short amount of time. libraries fully custom IO libraries can be created in an amazingly short amount of time.

Product / Foundry proven IP

Certus has both IO template libraries and full featured IO libraries in a variety of processes including the 180nm, 130nm, 90nm, 65nm and 45nm nodes. These solutions are Si-proven in hundreds of products and in a variety of foundries world-wide including TSMC.

Benefits summary

- Highest confidence-level for first time-right IC ESD Design due to SPICE simulation, optimization and verification methodology including HBM, MM, CDM specifications
- Most area efficient solution allow for IO height reduction of typically more than 20% compared to standard foundry IOs
- Portable & foundry proven including TSMC
- Si product proven IP in most advanced CMOS from 180nm down to 45nm
- Uniform ESD protection levels with more effective CDM protection
- Standard, full custom libraries plus IO template library offering
- Enabling of short-time custom IO library design



Certus IO cell shrink compared to standard IO cell typically > 20%